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23. (Three Times Amended) A semiconductor device comprising:

a semiconductor substrate;

a barrier film comprised of elemental barium atoms, having a thickness in the range of approximately 5 Å to approximately 100 Å on said substrate; and

a metallic material positioned on said barrier film such that said elemental barium atoms are between said metallic material and said semiconductor substrate.

REMARKS

Claims 1-13, 21 and 23-28 are currently pending in the present application. Claims 2 and 23 have been amended. The Examiner's indication that claims 1, 21 and 27 are allowed is acknowledged with appreciation.

In the above amendment, claim 2 has been amended to recite that the substrate is a semiconductor substrate and to require that the barrier film be directly on the semiconductor substrate. Claim 23 has been amended to require that the barrier film comprise elemental barium atoms.

In addition, claims 2 and 23 have been amended to clearly recite that the elemental barrier atoms are between the conductor and the semiconductor substrate in order to more clearly emphasize the differences between the present invention and the structure disclosed in Tsukamoto et al.

Claims 2-13, 23-26 and 28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,962,921 (Farnworth et al.). This rejection, at least insofar as it applies to claims 2-13, 23-26 and 28, as amended, is respectfully traversed and reconsideration is requested for the reasons which follow.

The present invention, as recited in claim 2 and claims dependent therefrom, requires at least a semiconductor device including a semiconductor substrate, a barrier film directly on said substrate and a conductor on said barrier film. The barrier film has a layer comprising barium atoms on said surface. The conductor is a conductor which has a tendency to diffuse into said substrate material if in direct contact therewith.

The present invention offers the advantage of providing a barrier film that is effective to inhibit diffusion of materials such as conductors, especially materials such as copper, into adjacent semiconductor substrates.

The present invention, as recited in claim 23 and claims dependent therefrom, requires a semiconductor substrate, a barrier film comprising barium atoms having a thickness in the range of approximately 5 Å to approximately 100 Å on said semiconductor substrate and a metallic material on the barrier film. This embodiment of the invention provides an extremely thin barrier film, which prevents diffusion of the metallic material into the semiconductor substrate. As is recognized by persons skilled in the art of chip manufacture, the thickness of each individual component or layer in a chip is critical to the performance of the chip since the greater the thickness of a particular component or chip, the farther an electrical signal must travel between layers. This additional travel distance reduces chip performance and increases the heat generated by the chip due to electrical resistance in the conductive material, both of which are important disadvantages in the field of chip manufacture.

Farnworth et al. does not address the problem solved by the present invention, namely, to permit the use of conductors in chip manufacture, such as copper, which tend to diffuse into semiconductor substrates. A skilled person confronted with this problem and armed with the teachings of Farnworth et al. would have no idea how to solve the problem.

The Examiner takes the position that Farnworth et al. discloses all of the features of claim 2 of the present application except for the thickness of the barrier layer. This statement is not understood in relation to claim 2 since there is no limitation as to the thickness of the barrier layer contained in claim 2. The Examiner's position is apparently that in Figs. 3A-3C of Farnworth et al., materials 30, 36 are the same as the presently claimed substrate, conductor 34 is the same as the presently claimed barrier layer and solder bumps 12 are the same as the presently claimed conductor. The applicant respectfully disagrees for the reasons set forth below.

Farnworth et al. lacks a disclosure of several important features of claim 2, as amended. First, claim 2 now requires that the barrier film be directly on the semiconductor substrate. As can be clearly seen from Figs. 3A-3C of Farnworth et al., the conductor 34 is not located directly on the semiconductor substrate. Instead, Farnworth et al. clearly teaches that there is an insulating layer 36 between the

semiconductor substrate 30 and the conductor 34. Thus, this limitation of claim 2, as amended, is not taught or suggested by Farnworth et al.

Secondly, Farnworth et al. does not disclose that the conductor 34 is elemental barium. Rather, Farnworth et al. makes a list of 29 possible materials which can be included in the conductor 34, one of which is barium. However, Farnworth et al. does not specify that barium, if included in the conductor 34, is elemental barium nor does Farnworth et al. contain an example of elemental barium. Rather, Farnworth et al. mentions several possible forms for the 29 materials listed as possible materials for the conductor. The 29 listed materials, including barium, can be in any one of the following forms: 1) As a plated or metallized material, 2) as an alloy, 3) in combination with other elements. Farnworth et al. does not specify the form in which barium is employed.

The conductor 34 of Farnworth et al. could only meet the limitations of the barrier film of claim 2 if it were plated or metallized. However, the U.S. Patent 5,607,818 incorporated by reference by Farnworth et al. for teaching the metallization process at col. 8, lines 5-8 of Farnworth et al. does not suggest plating or metallization of elemental barium nor does it teach a process for use in plating or metallization of barium nor does it even mention barium. In fact, Farnworth et al does not teach or suggest the desirability of applying a thin layer of elemental barium to a substrate nor does Farnworth et al. teach a method for applying a thin layer of elemental barium to a semiconductor substrate and thus the rejection is insufficient because none of the cited references enables a skilled person to provide the claimed elemental barium layer. A reference must be enabling for all features of the claimed invention. Accordingly, Farnworth et al. does not disclose a layer of elemental barium nor does Farnworth et al. enable a skilled person to apply a layer of elemental barium.

Finally, Farnworth et al. does not teach or suggest the provision of a layer of conductive material on said barrier film wherein the conductive material <u>has a tendency to diffuse into the semiconductor substrate</u>. The only material Farnworth et al. discloses for application to the conductor 34 is a lead/tin alloy, which is 95% lead and 5% tin. The Examiner has not demonstrated that this is a material that has a tendency to diffuse into a semiconductor substrate. This is also not one of the materials listed in the specification of the present application that has a tendency to diffuse into a semiconductor substrate.

Furthermore, it would not be an obvious matter of design choice to substitute another conductive material for the lead/tin alloy since Farnworth et al. only suggests using some form of barium with a lead/tin alloy solder because it is important to use a material that is not reactive with lead/tin alloy solder (col. 7, line 66 to col. 8, line 3 of Farnworth et al). If lead/tin alloy solder is replaced by another material, then a skilled person would follow the teaching of Farnworth et al. at col. 7, lines 54-57 to use a highly conductive metal instead of, for example, a form of barium. The highly conductive metals listed in Farnworth et al. are aluminum, gold, iridium, copper, tungsten, tantalum, molybdenum and alloys of these metals. Accordingly, Farnworth et al. lacks this feature of claim 2 as well.

According to MPEP § 2143.03 the combination of references used in a rejection under 35 U.S.C. § 103(a) rejection must disclose all of the features of the claimed invention. As shown above, at least three features of the invention of claim 2 are not taught or suggested by Farnworth et al. nor are these features within the common knowledge of a person of ordinary skill in the art and thus this rejection is insufficient and should be withdrawn.

With respect to claim 23, Farnworth et al. again lacks a teaching of a layer of elemental barium for the reasons discussed above. In addition, Farnworth et al. does not teach or suggest that the conductor layer should have a thickness of approximately 5 Å to approximately 100 Å. The Examiner considers that this thickness is an obvious design choice because, in the Examiner's opinion, changes in the thickness of the layer would produce no functional differences. This is not correct.

This embodiment of claim 23 provides an extremely thin barrier film, which prevents diffusion of the metallic material into the semiconductor substrate. As is recognized by persons skilled in the art of chip manufacture, the thickness of each individual component or layer in a chip is critical to the performance of the chip since the greater the thickness of a particular component or chip, the farther an electrical signal must travel between layers. This additional travel distance reduces chip performance because signals take longer to reach their destination and increases the heat generated by the chip due to electrical resistance in the conductor, both of which are important disadvantages in the field of chip manufacture. Thus, the extremely thin film layer of the

present invention provides significant functional benefits when employed in semiconductors.

Moreover, it is improper for the Examiner to allege that the provision of a film of elemental barium having a thickness of approximately 5 Å to approximately 100 Å is an obvious design choice when the Examiner has not cited a single reference which teaches or suggests a process which can be used by a skilled person to apply such a thin layer of elemental barium to a substrate. If a skilled person does not even know how to make such a layer of elemental barium on a semiconductor substrate, it cannot be an obvious design choice to make a layer of elemental barium having the claimed thickness. Until the Examiner substantiates the position that it is possible using a known prior art method to prepare such a thin layer of elemental barium on a semiconductor substrate it is improper to allege that the claimed thickness is an obvious design choice and this rejection should be withdrawn.

All of the remaining claims depend from one of claims 2 and 23 and thus at least the same arguments apply to all of these claims. For the foregoing reasons, the rejection under 35 U.S.C. § 103(a) over Farnworth et al. should be withdrawn.

Claims 2-13, 23-26 and 28 have been rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 5,285,079 (Tsukamoto et al.). This rejection, at least insofar as it applies to claims 2-13, 23-26 and 28, as amended, is respectfully traversed and reconsideration is requested for the reasons which follow.

It is important to note that Tsukamoto et al. does not address the problem solved by the present invention, namely, to permit the use of conductors, such as copper, which tend to diffuse into semiconductor substrates. A skilled person confronted with this problem and armed with the teachings of Tsukamoto et al. would have no idea how to solve the problem.

With respect to claim 2, the Examiner again alleges that Tsukamoto et al. discloses all of the claimed limitations except for the thickness of the barrier layer. Again this is not understood since the thickness of the barrier layer is not a limitation of claim 2. The Examiner apparently takes the position that elements 101-104 of Tsukamoto et al. are the same as the presently claimed substrate, element 105 of Tsukamoto et al. is the same as the presently claimed barrier film and element 106 is the same as the presently

claimed conductor. The applicant respectfully disagrees, at least insofar as the rejection applies to the claims, as amended.

Claims 2-13, 23-26 and 28, as amended, clearly distinguish over the device of Tsukamoto et al. As discussed in the remarks to the Amendment dated September 7, 2000, Tsukamoto et al. does not teach the provision of elemental barium between a semiconductor layer and a conductor, which has a tendency to diffuse into the barrier layer. Instead, Tsukamoto et al. teaches the provision of a substrate onto which a collector layer 105 of a semiconductor material is applied. Then, ohmic contact electrodes 106 are applied atop a portion of the collector layer 105 of semiconductor material as shown, for example, in Fig. 1.

Most importantly, Tsukamoto et al. teaches that it may be useful to provide a surface coating of a material, which may be cesium or barium to the areas of the surface which emit electrons. See col. 3, lines 46-49. The areas of the surface that emit electrons are the exposed surface areas of the collector layer 105, which have not been covered with the ohmic contact electrodes 106. Thus, since the layer that may be barium, is applied after the ohmic contact electrodes 106 have already been applied to the top of the collector layer 105 of semiconductor material, the barium of Tsukamoto is not located between the ohmic contact electrodes 106 and the semiconductor substrate. Instead, in the device of Tsukamoto et al. the barium would be located on the surface of collector layer 105 around the ohmic contact electrodes106. Thus, although the layer, which may be barium forms part of collector layer 105, it is not located between the ohmic contact electrodes 106 and the semiconductor substrate as is now required by the amended claims of the present application.

Since Tsukamoto et al. specifically teaches that the coating which may be barium should be applied to the electron emitting areas of the collector layer 105, Tsukamoto et al. clearly teaches away from the present invention since the areas between collector layer 105 and ohmic contact electrodes 106 of Tsukamoto et al. are not electron emitting areas of the collector layer 105.

For the foregoing reasons, the rejection of claims 2-13, 23-26 and 28 under 35 U.S.C. § 103(a) should be withdrawn. Favorable consideration, entry of the amendment, and issuance of a Notice of Allowance are respectfully requested.

If the Examiner believes that a telephone conference would be useful to expedite the prosecution of this application, the Examiner is invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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I hereby certify that this paper (along with any attachments or enclosures) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner of Patents, Washington, D.C.

Date: April 26, 2001

Beverly D. Cook

Marked-Up Version of Claims 2 and 23 Showing Amendments

2. (Four Times Amended) A semiconductor comprising:

a semiconductor substrate material having a surface;

a barrier film directly on said semiconductor substrate surface, said barrier film having a layer comprising elemental barium atoms on said surface;

a conductor on said barrier film, said conductor having a tendency to diffuse into said semiconductor substrate material if in direct contact therewith; and wherein said elemental barium atoms are between said conductor and said semiconductor substrate such that said layer [comprising elemental barium atoms] serves as a barrier, inhibiting diffusion of the conductor into the semiconductor substrate material.

23. (Three Times Amended) A semiconductor device comprising:

a semiconductor substrate;

a barrier film comprised of elemental barium atoms, having a thickness in the range of approximately 5 Å to approximately 100 Å on said substrate; and

a metallic material positioned on said barrier film such that said elemental barium atoms are between said metallic material and said semiconductor substrate.